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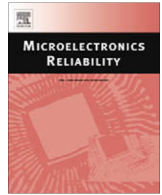

Finite element modeling on electromigration of solder joints in wafer level packages

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ABSTRACT

This work studies the electromigration of solder joints in an encapsulated copper post wafer level package (WLP) by finite element modeling. Experimental data showed that the electromigration failure occurs in solder joints on the printed circuit board (PCB) side due to the current crowding. In order to improve the electromigration performance on the PCB side with a copper post WLP, two new line-to-bump geometry designs are proposed. Coupled electro-thermal finite element modeling is performed to obtain the electrical and thermal fields simultaneously. The ionic flux from electron wind and thermal response is calculated based on finite element solutions. The divergence of the total flux, which is the sum of the divergence of electromigration and thermomigration, is extracted at the critical locations in solder joints. Results show that the new proposed design structures can reduce the maximum current density by 19%, and the divergence of the total ionic flux by 42%. Thermal gradient is very small in solder joints, therefore, the main driving force for electromigration failures comes from the electron wind. The finite element results on mesh dependency are discussed in this paper.

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1. Introduction

Electromigration is defined as mass transport due to momentum exchange between conducting electrons and diffusing metal atoms when a high electrical current density is applied. It can cause progressive damage to metal conductors in an integrated circuit (IC). As electronics industry continues to push for high performance and the miniaturization of electronic devices, the demand for high current density may cause electromigration failures not only in IC interconnects such as in Al or Cu traces, but also in solder bumps [1–3]. Several key differences exist between electromigration in Cu vs. Al vs. solder metallurgical systems [4]. Since electromigration is electron wind assisted diffusion related process, the underlying dominant diffusion mechanism plays a key role in governing the kinetics of electromigration. In Cu, the predominant diffusion mechanism at typical operating temperatures is surface diffusion. In Al, it is expected to be grain boundary diffusion. However, in solders, which have low melting temperatures, the predominant diffusion mechanism is lattice diffusion. In addition, solder systems are very complex metallurgical systems. The dissolution of solutes from substrate or package barrier layers (Cu, Ni, Pd, Au) into solder during reflow makes the solder alloys extremely complex multi-component thermodynamic system. The solute elements dissolved in the solder are typically interstitial in nature and hence diffuse substantially fast in solder matrix. Additionally, solders are typically multiphase alloys and undergo several intermetallic reactions at interfaces. Furthermore, the resistivity of solders is an order of the magnitude higher than Al and Cu interconnects. Consequently, the electromigration behavior of solder materials provides several challenges as compared to Al and Cu interconnects [4].

Zhang et al. [2] studied the effect of current crowding on void propagation at the interface between intermetallic compound (IMC) and solder in a chip scale wafer level package with an under bump metallization (UBM) layer. The average current density in solder joints has reached 10^4 A/cm^2. Due to the line-to-bump geometry in an UBM configuration and high homologous temperature, the electromigration behavior in solder joints is uniquely dominated by current crowding at the cathode contact of a solder bump where a very large change of current density occurs. The typical failure mode is the propagation of a pancake-type of void across the cathode contact interface.

It is understood that solder joint thermo-mechanical reliability performance become a critical concern of WLPs with larger die packages. Copper post wafer level packages have demonstrated superior thermo-mechanical reliability performance [5]. Instead of using UBM structure to connect solder bumps, a thick copper pillar is electroplated, followed by an epoxy encapsulation before solder attachment in a copper post WLP package. Liu et al. [4] studied the electromigration failures of copper pillar flip chip configurations with both SnPb and SnAg (Ag-3.5) alloys. It has been proposed that there are two driving forces for electromigration failure in solder bumps. One is Sn consumption that can generate

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extra vacancies. The other is electron wind that can move the predominant diffusion species from the cathode to the anode side. In SnPb alloy, Pb is the dominant diffusion species at the testing temperature (165 °C). Its diffusion direction follows the electron flow direction from substrate side to die side due to the momentum exchange between electron wind and Pb atoms in solder alloy, and Sn will move in the opposite direction to fill the vacancies formed by Pb flux. In SnAg solder, Sn is the dominant diffusion species. Its microstructure is mainly Sn matrix plus Ag_3Sn intermetallic compound. Electron wind moves Sn away from the cathode side to the anode side and causes electromigration failure.

Compared to an UBM WLP structure with a copper post WLP structure, the failure location due to electromigration is different. In an UBM configuration, current crowding occurs at the cathode contact of a solder bump, in the region just adjacent to the UBM layer. While in a copper post WLP structure, current crowding occurs at a solder bump on PCB side. Figs. 1 and 2 show the typical failure locations of a UBM WLP and a copper post WLP, respectively.

In this paper, electromigration failures in a copper post wafer level package are studied by the coupled thermal–electrical finite element modeling. The existing line-to-bump structure is modeled first to compare with the experimental results. Two new

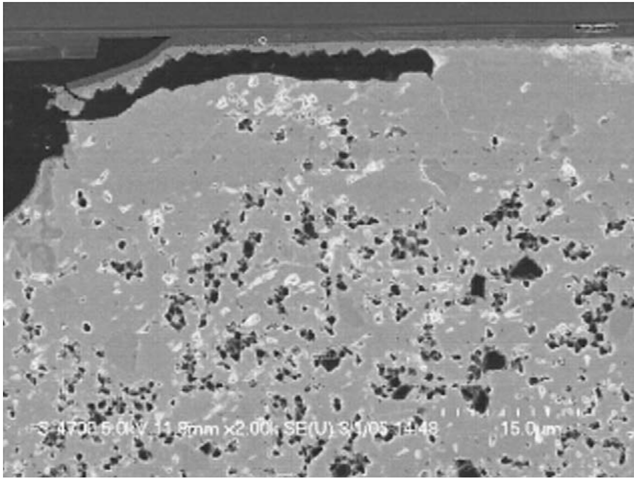

Fig. 1. Electromigration-induced voiding in a wafer level package with UBM layer [2].

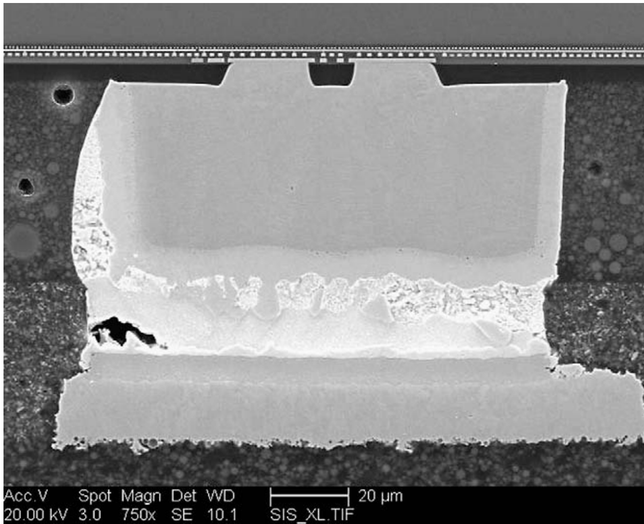

Fig. 2. Electromigration-induced voiding in a copper pillar flip chip package [4].

line-to-bump structures are proposed to improve the electromigration performance for copper post WLP packages. Detailed finite element modeling is carried out with new designs to investigate the current density distribution and temperature distribution. Since flux divergence is eventually responsible for void nucleation and formation, a post-processing script is developed to calculate the total atomic flux divergence due to electrical and thermomigration. The results for the test structure with the proposed new line-to-bump design are studied, and compared with the results with the existing design.

2. Mathematical formulation of electromigration

In general, the total atomic flux divergence is a sum of individual atomic flux divergence because of electromigration, thermomigration, and stress-migration. This can be expressed as follows [6]

$$\mathrm{div}(\vec{J}_{Tot}) = \mathrm{div}(\vec{J}_{Em}) + \mathrm{div}(\vec{J}_{Th}) + \mathrm{div}(\vec{J}_{s}) \tag{1}$$

where

$$\mathrm{div}(\vec{J}_{Em}) = \left(\frac{E_A}{K_BT} - \frac{1}{T} + \alpha\frac{\rho_0}{\rho}\right)\cdot \vec{J}_{Em}\cdot\nabla T + \frac{1}{N}\nabla N \tag{2}$$

$$\mathrm{div}(\vec{J}_{Th}) = \left(\frac{E_A}{K_BT^2} - \frac{3}{T} + \alpha\frac{\rho_0}{\rho}\right)\cdot \vec{J}_{Th}\cdot\nabla T + \frac{NQ^*D_0}{3K_B^3T^3}j^2\rho^2e^2\exp\left(-\frac{E_A}{K_BT}\right) + \frac{1}{N}\vec{J}_{Th}\cdot\nabla N \tag{3}$$

$$\mathrm{div}(\vec{J}_{s}) = \left(\frac{E_A}{K_BT^2} - \frac{1}{T}\right)\cdot \vec{J}_{s}\cdot\nabla T + \frac{1}{N}\vec{J}_{s}\cdot\nabla N - \frac{2N\Omega D_0E\alpha_l}{3K_BT(1-\nu)} \times \exp\left(-\frac{E_A}{K_BT}\right)\left\{\frac{j^2\rho^2e^2}{3K_B^2T} + \left(\frac{1}{T} - \alpha\frac{\rho_0}{\rho}\right)\nabla^2T\right\} \tag{4}$$

The theoretical expression to calculate the total atomic flux divergence, taking into account electromigration, thermomigration, and stress-migration is then given as follows,

$$\begin{aligned}\mathrm{div}(\vec{J}_{Tot}) = {} & \left(\frac{E_A}{K_BT} - \frac{1}{T} + \alpha\frac{\rho_0}{\rho}\right)\cdot \vec{J}_{Em}\cdot\nabla T + \left(\frac{E_A}{K_BT^2} - \frac{3}{T} + \alpha\frac{\rho_0}{\rho}\right) \\ & \cdot \vec{J}_{Th}\cdot\nabla T + \frac{NQ^*D_0}{3K_B^3T^3}j^2\rho^2e^2\exp\left(-\frac{E_A}{K_BT}\right) \\ & + \left(\frac{E_A}{K_BT^2} - \frac{1}{T}\right)\cdot \vec{J}_{s}\cdot\nabla T - \frac{2N\Omega D_0E\alpha_l}{3K_BT(1-\nu)} \\ & \times \exp\left(-\frac{E_A}{K_BT}\right)\left\{\frac{j^2\rho^2e^2}{3K_B^2T} + \left(\frac{1}{T} - \alpha\frac{\rho_0}{\rho}\right)\nabla^2T\right\}\end{aligned} \tag{5}$$

where N is the atomic concentration, e is the electron charge, $\vec{J}$ corresponds to the local current density vector, ρ is the temperature dependant value of electrical resistivity ($\rho = \rho_0(1 + \alpha(T - T_0))$), D_0 is the self diffusion-coefficient of the conductor material, K_B is the Boltzmann constant, T is the value of the local temperature, Z^* represents the effective charge of ions, Ω is the atomic volume, E is Young modulus, α_l coefficient of thermal expansion, α is the thermal coefficient of resistivity, Q^* is the specific heat of transport, E_A is the activation energy of the material, $\vec{J}_{Em}$, $\vec{J}_{Th}$, and $\vec{J}_S$ are the atomic flux due to electromigration, thermomigration and stress-migration, respectively. $\vec{J}_{Em}$, $\vec{J}_{Th}$, and $\vec{J}_S$ can be expressed as follows [7]

$$\vec{J}_{Em} = \frac{N}{K_BT}eZ^*\vec{J}\rho D_0\exp\left(-\frac{E_A}{K_BT}\right) \tag{5a}$$

$$\vec{J}_{Th} = \frac{NQ^*D_0}{K_BT^2}\exp\left(-\frac{E_A}{K_BT}\right)\nabla T \tag{5b}$$

$$\vec{J}_{s} = -\frac{N\Omega D_0}{K_BT}\exp\left(-\frac{E_A}{K_BT}\right)\nabla\sigma_H \tag{5c}$$

where σ_H is the local hydrostatic stress value $\sigma_H = (\sigma_{xx} + \sigma_{yy} + \sigma_{zz})/3$), where σ_{xx}, σ_{yy} and σ_{zz} correspond respectively to the normal components provided by the local stress tensor.

In order to calculate the total divergence, the distribution of $\vec{J}$, the current density vector, T, the absolute temperature, and ∇T, the temperature gradient, must be obtained first. The coupled thermal–electrical governing equations can be expressed as follows,

$$-\nabla \cdot ((\rho_0(1+\alpha(T-T_0)))\nabla V) = 0$$
$$\rho_t C\frac{\partial T}{\partial t} - \nabla \cdot (k\nabla T) = \frac{1}{\rho}|\nabla V|^2 \quad (6)$$

where ρ_t is the density, C is heat capacity, T is temperature, k is thermal conductivity, V is the electrical potential, α is thermal coefficient of resistivity and ρ is the electric resistivity. The basic variables in those equations are temperature T and electrical potential V. They are coupled each other since material's resistivity is temperature-dependent, and, on the other hand, the joule heating, expressed by the right side term of the second Eq. (6), introduces the redistribution of temperature. In our present study, temperature field is assumed to be steady-state.

To simplify the problem, only the phenomenon of electromigration and the thermomigration are considered in this work. In this case, the total divergence in the atomic flux becomes

$$\mathrm{div}(\vec{J}_{Tot}) = \left(\frac{E_A}{K_B T} - \frac{1}{T} + \alpha\frac{\rho_0}{\rho}\right) \cdot \vec{J}_{Em} \cdot \nabla T + \left(\frac{E_A}{K_B T^2} - \frac{3}{T} + \alpha\frac{\rho_0}{\rho}\right) \cdot \vec{J}_{Th} \cdot \nabla T + \frac{NQ^* D_0}{3K_B^3 T^3} j^2 \rho^2 e^2 \exp\left(-\frac{E_A}{K_B T}\right) \quad (7)$$

Fig. 3 gives the flow chart to describe the analysis procedure in this work. ANSYS 11.0 Multiphysics is used. Solid5 3-D solid element, which is a directly coupled electrical, thermal and structural element, is applied. Post-processing scripts are developed using ANSYS APDL code to calculate the flux component using Eqs. (5a) and (5b). Finally, the total divergence is calculated by Eq. (7).

3. Line-to-bump geometry designs

Encapsulated copper post wafer level packaging technology has been developed recently to improve solder joint thermo-mechanical reliability under thermal cycling. For a copper post WLP, UBM layer is not needed. Instead, a thick copper post is electroplated, followed by an epoxy encapsulation, as shown in Fig. 4. Studies on these structures have shown that there is an intrinsic current crowding region at lower corner of solder balls, as shown in Fig. 2. This implies that electromigration failure may shift from the upper corner in UBM WLP structure to the lower corner in copper post WLP structure. To reduce the electromigration at the PCB side, two new designs of line-to-bump geometry are proposed for the lower interconnects, as shown in Fig. 5.

In the new Design A (see Fig. 5a), the current enters solder bumps in the middle region of the bumps through a copper trace first, and is then spread into the bulk of solder bumps. It is expected that this design will reduce the magnitude of current density; therefore, the risk of electromigration failures can be reduced. In the new Design B, a thick copper trace structure is designed for

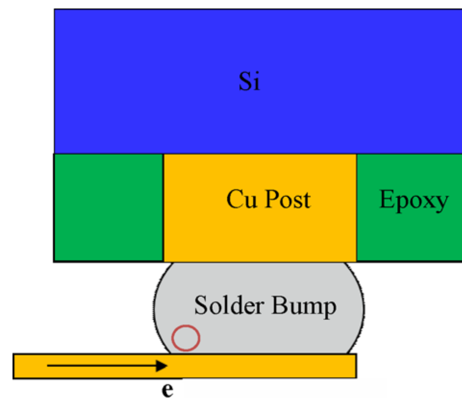

Fig. 4. Intrinsic current crowding region in a copper post wafer level package.

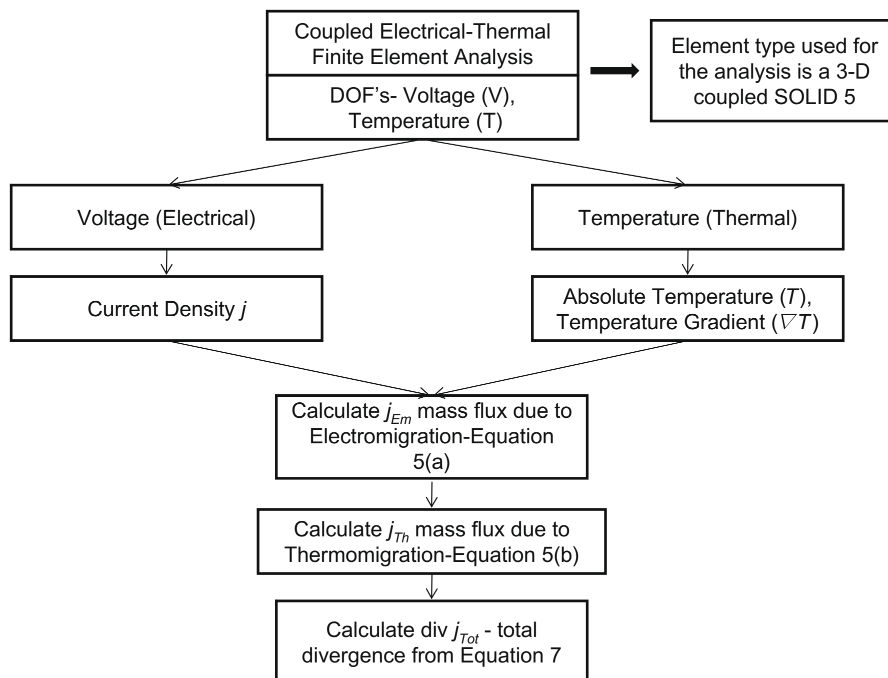

Fig. 3. Flowchart of electro-thermal finite element modeling procedure.

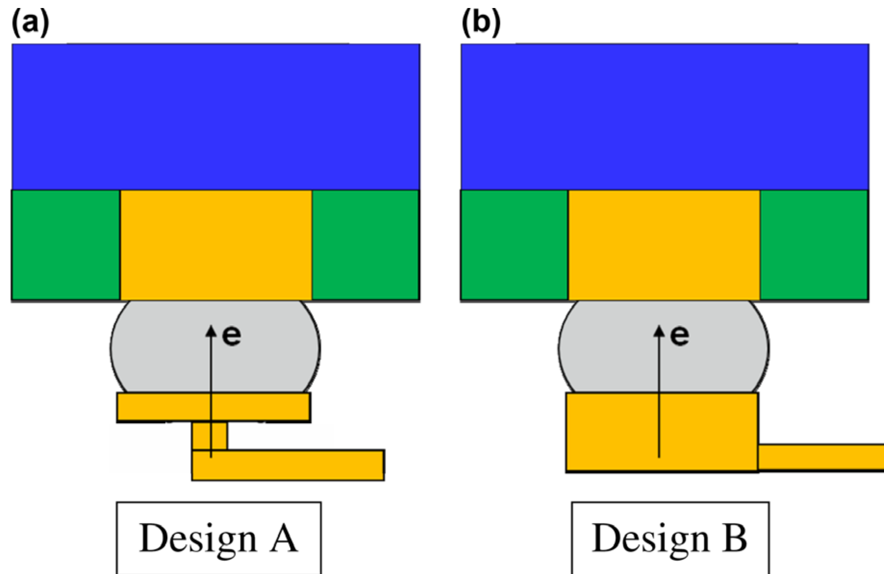

Fig. 5. Schematics of two new line-to-bump structures.

interconnections on the PCB side (see Fig. 5b). So the current enters the copper post and distribute itself evenly through it and further into the solder bump.

4. Finite element modeling

The package chosen for the analysis is a copper post wafer level package, which has a 6 × 6 solder ball array with 0.5 × 0.5 mm solder ball pitch [8]. The exterior 20 balls are assumed to connect with each other in a daisy chain for study. The components used in the system include: silicon chip, Cu trace, Cu post/bump, epoxy, solder bumps, and the PCB. Because of the symmetry of the package, the quarter models with 3 × 3 ball array can be used for the analysis, as shown in Fig. 6. In this model, only five bumps are electrically connected.

Finite element models with the existing and proposed line-to-bump designs are shown in Figs. 7 and 8a, respectively. In the proposed test structure two different line-to-bump designs are included. The Design A, which was discussed in the earlier section, is used for the connection of Bumps 1 and 2, as shown in Fig. 8b and c. The Design B is used for the connection of Bumps 3 and 4, as shown in Fig. 8d and e.

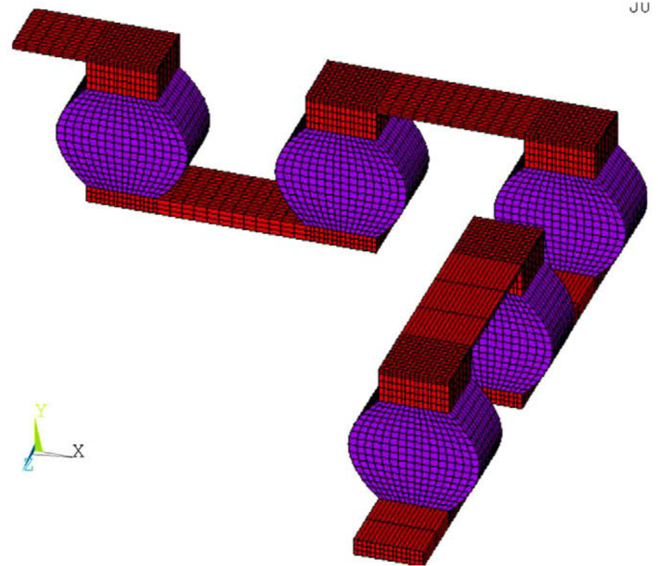

Fig. 7. Finite element model of the existing line-to-bump design.

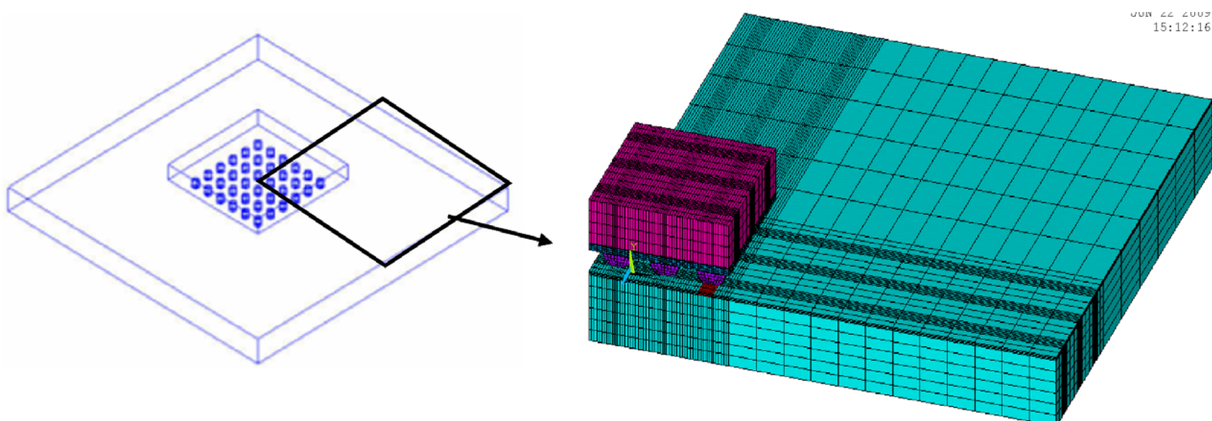

Fig. 6. The quarter model due to symmetry.

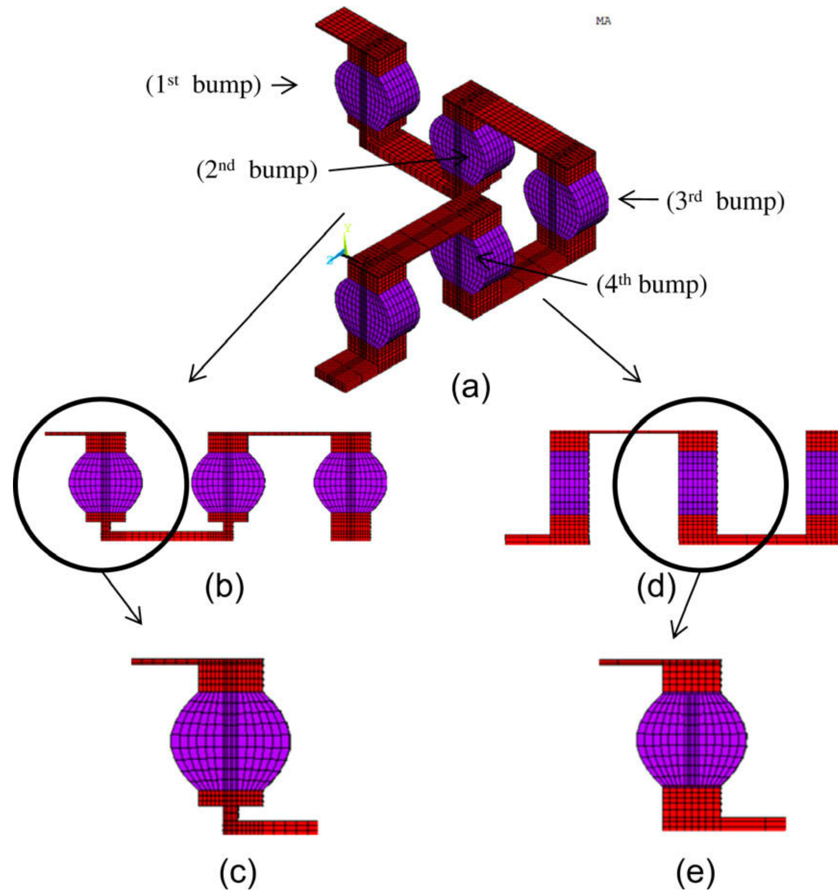

Fig. 8. (a) Finite element model of the proposed line-to-bump designs A and B; (b) the proposed design A (connecting bumps 1 and 2); (c) detailed view of design A; (d) the proposed design B (connecting bumps 3 and 4) and (e) detailed view of design B.

An electrical voltage difference is applied between the ends of the Cu traces at the chip side and the PCB side, with a current load of −1.7 amps (−ve) applied at the end of the Cu trace on the chip side. The effect by joule heating increases the temperatures of the whole structure. The ambient temperature surrounding the test structure is 50 °C, so there will be a convective heat transfer between the structure and ambient air. The convective heat transfer coefficient is 20 W/m^2 °C.

The electromigration parameters for SnAgCu solder bump are listed in Table 1 [3,9–14] where E_A is activation energy, Z^* is effective charge number, D_0 is self diffusion-coefficient, Q^* is heat of transport, ρ_0 is initial electrical resistivity, α is temperature coefficient resistance, Ω is atomic volume, Boltzmann constant K_B is 1.380662e−23, the electron charge e is 1.60219e−19, and the room temperature T_0 is 303.

Thermal and electrical material properties are listed in Table 2. The electrical resistivity of the PCB and epoxy are assumed to be a very big number so that they are highly resistive to conduct electricity.

Table 1
Electromigration basic parameters [3,9–14].

Parameter	Units	Value
E_A	eV	0.8
Z^*	–	−23
D_0	m^2/s	0.027
Q^*	eV	0.0094
ρ_0	Ω m	13.3e−8
α	1/K	2.8e−3
Ω	m^3/atom	2.72e−29

Table 2
Material properties for numerical analysis.

Material	Material properties		
	Specific heat (J/kg K)	Thermal conductivity (W/m K)	Electrical resistivity (Ω m)
PCB	–	1.7	1e10
Solder (SAC)	219	57.26	13.3e−8(1 + 2e−3ΔT)
Silicon die	–	150	4.4
Copper	385.2	393	1.58e−8(1 + 4.3e−3ΔT)
Epoxy	2185	1.2	1e17

5. Results

5.1. Current density

The current crowding, which occurs when there is a sudden change in the cross-section area, is the main cause for the electromigration. Fig. 9 shows the current density distribution in the solder bumps with the existing line-to-bump geometry design. From the figure, it can be seen that the current crowding occurs at the nearest corner at which a large portion of the current enters or leaves the solder bump. Such results are consistent with the experimental observations, as shown in Fig. 2. The current density at the corner is approximately one order of the magnitude higher than the average current density in solder bumps. The third bump in

the center is the risky bump with a maximum current density of 0.139e9 A/m^2.

Fig. 10 shows the current density distribution of the proposed line-to-bump geometry designs. Since the current enters the bumps from the middle portion of the bumps, the current density is reduced significantly in the lower regions. This can be clearly seen from the vector plot in Fig. 10. However, the maximum current density location is now on chip side, as shown in Fig. 11, with a maximum value of 0.113e9 A/m^2, observed in the fourth bump which is connected by Design B. The bumps connected by Design A have current densities less than the maximum density.

Table 3 lists the maximum current density values for Design B compared to the existing design. There is a decrease by 18.7%.

It has been found that the bumps connected by Design A perform well in reducing the maximum current density. So, the second bump connected with Design A in the proposed structure is

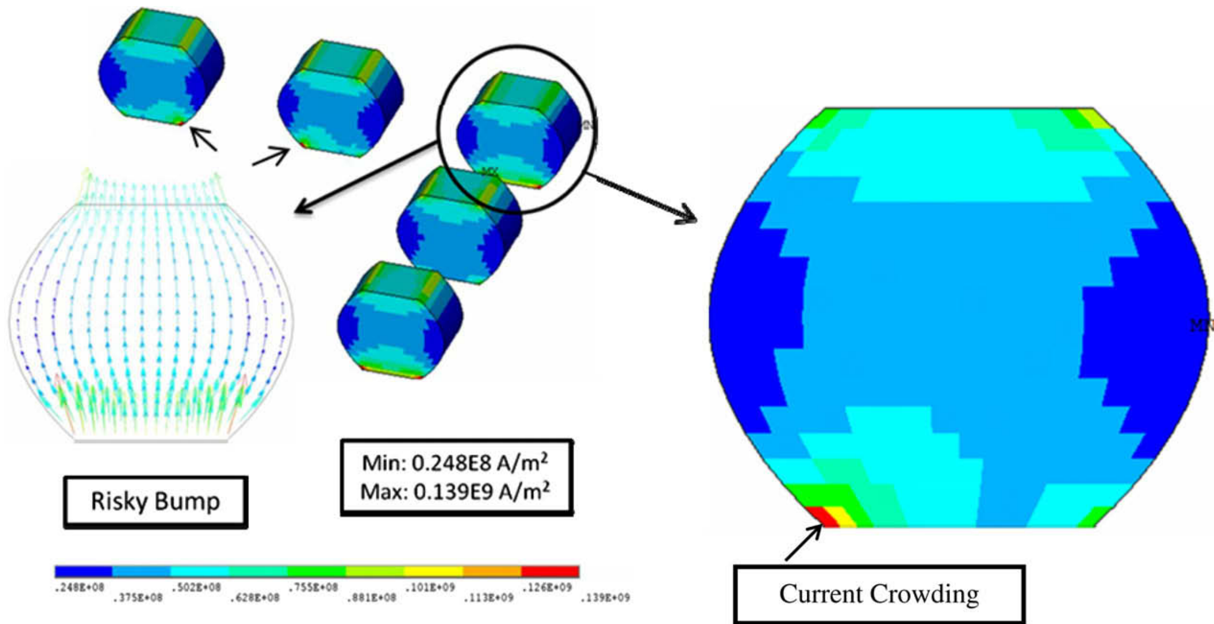

Fig. 9. Current density contour plot with the existing design.

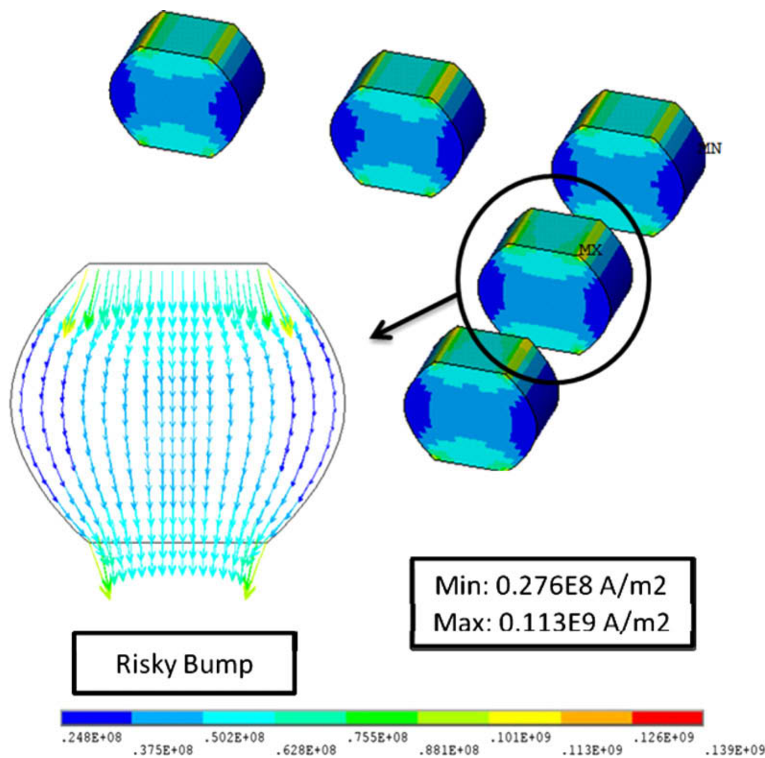

Fig. 10. Current density contour plot with the proposed designs.

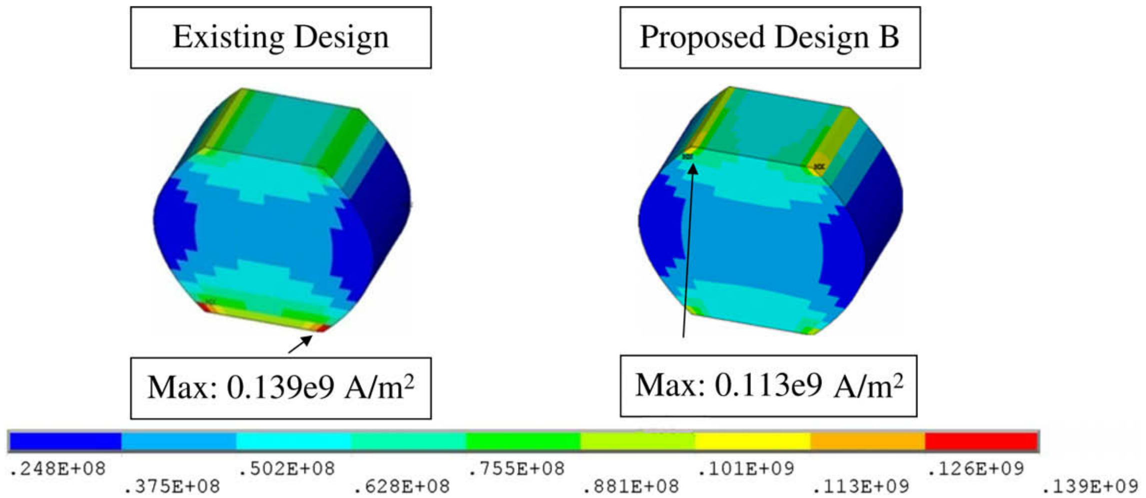

Fig. 11. Comparison of the maximum current density for the existing and proposed design B.

Table 3
Percentage decrease in current densities in terms of maximum current density.

	Current density (A/m^2)
Existing design	0.139e9
Proposed design B	0.113e9
% Decrease	18.71

Table 4
Percentage decrease in current densities at lower corner of 2nd bumps.

	Current density (A/m^2)
Existing design	0.139e9
Proposed design A	0.95e8
% Decrease	31.65

compared to the second bump connected with the existing design in the present structure. The second bump with the existing design has maximum current density at the bottom left corner, similar to the second bump with the proposed design, as shown in Fig. 12. Table 4 shows a percentage decrease of the current density by 31.65% in the bump with proposed Design A.

5.2. Temperature distribution

Fig. 13 shows the temperature distribution in the bumps. The minimum and maximum temperatures in the bumps are 391.6 K and 392.8 K, respectively, in the case of the existing design. They are 392.9 K and 394.2 K, respectively, for the package with the proposed design. Because of the presence of very small thermal gradient in each design, the induced divergences due to thermomigration would be very small.

5.3. Mesh dependency

Since the results of a finite element model depends on mesh density, it is important to choose the appropriate mesh density to obtain the accurate results. In this work different mesh schemes are considered and their corresponding maximum current densities are obtained. The mesh scheme, from which the stabilization of maximum current density is observed, is chosen for meshing models. Table 5 shows that there is an increase in maximum current density with the increase in mesh density. For the structures with two, three, four times of the initial mesh densities there are large variations in the maximum current density. But for the structures with mesh densities greater than four times of the initial mesh density, the maximum current density appears to be stabilized with little variations. However, there might be a possibility that the singularity of current density exists at the corner of solder bumps.

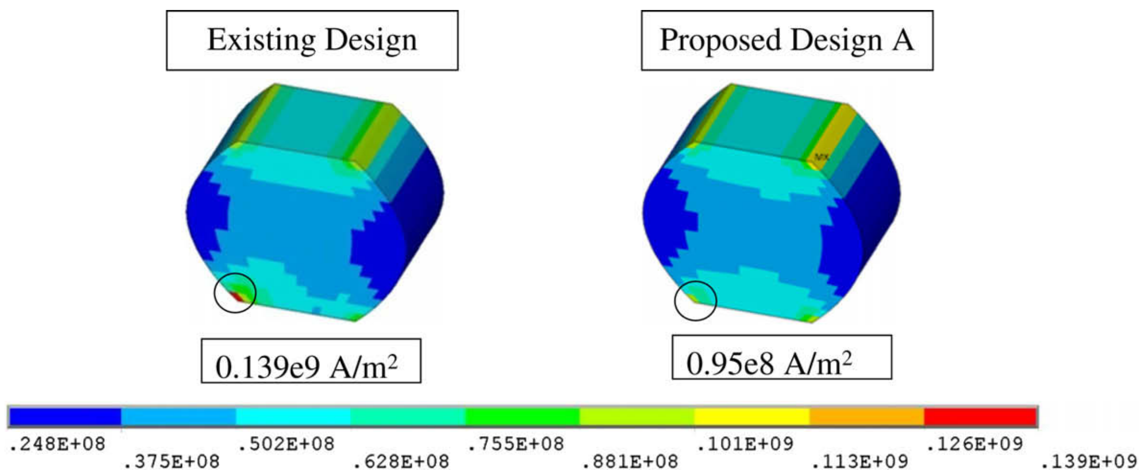

Fig. 12. Comparison of the current densities at the lower left corner of the bumps, with the existing and the proposed line-to-bump design A (2nd bumps).

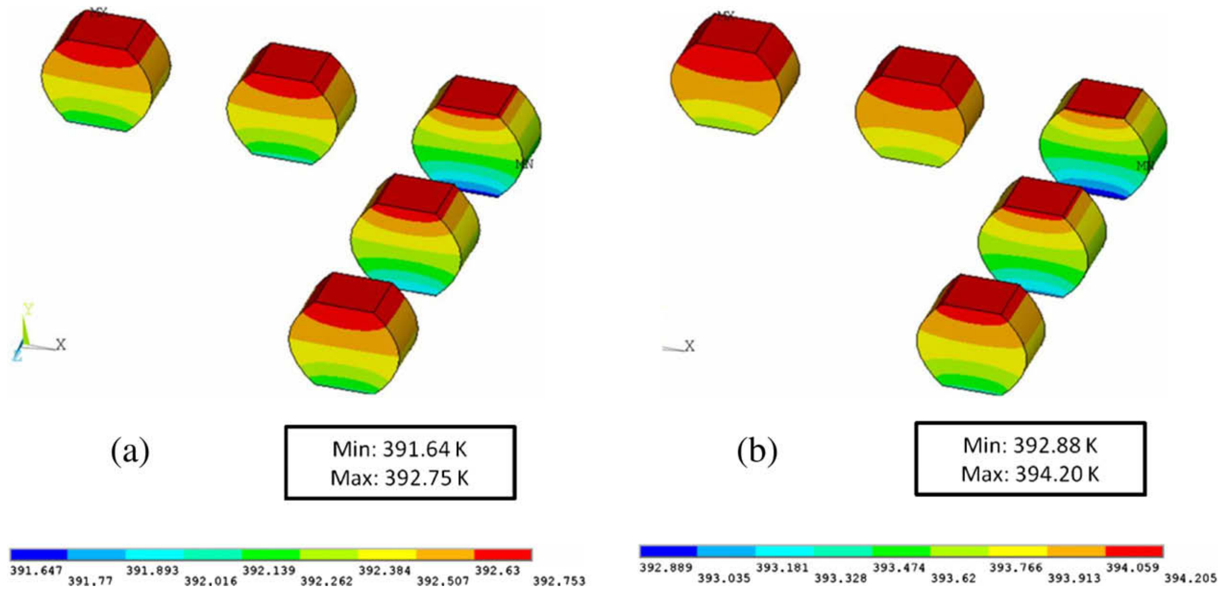

Fig. 13. Temperature distribution of the quarter model with (a) the existing line-to-bump design and (b) the proposed line-to-bump designs designs.

Table 5
Variation of maximum current density with the increase in mesh density.

Mesh density	Max. current density (A/m^2)
2 × Initial mesh	0.139e9
3 × Initial mesh	0.16e9
4 × Initial mesh	0.19e9
5 × Initial mesh	0.21e9
6 × Initial mesh	0.226e9

Table 6
List of divergence values comparing existing and proposed designs.

Design	div J_{Em}	div J_{Th}	div J_{Tot}	% Decrease
Existing	0.999E−5	0.266E−7	.1001E−4	
Proposed design A	0.574E−5	0.373E−7	0.577E−5	42
Existing	0.134E−4	0.528E−7	0.135E−4	
Proposed design B	0.111E−4	0.269E−7	0.114E−4	10

5.4. Divergence analysis

The values of current density and temperatures obtained through the coupled electrical-thermal analysis are used to calculate the massflow divergences due to electromigration (div J_{Em}, Eq. (2)) and thermomigration (div J_{Th}, Eq. (3)). The total massflux divergence (div J_{Tot}, Eq. (7)) is the sum of massflux divergence due to electromigration and thermal migration. The divergence values of the second and third bumps with the existing design are compared to the second bump with the proposed Design A and the third bump with the proposed Design B, respectively. The divergence values are listed in Table 6.

The comparison of these values reveals that the total divergence value of the second bump with the proposed Design A has decreased by about 42%; whereas in the third bump with the proposed Design B, the total divergence has decreased by 10%. Hence the proposed Design A is more significant in decreasing the divergence value when compared to proposed Design B.

6. Conclusions

The finite element modeling of a directly coupled electrical-thermal static analysis was performed to examine and quantify the effects of current crowding and joule heating in an encapsulated copper post wafer level package. For the structure with the existing line-to-bump design, the simulation results are consistent with the experimental results, which showed that the electromigration occurs in solder joints at PCB side where the maximum current density is generated. In order to reduce the risk of electromigration failures, new line-to-bump geometry designs are proposed. Finite element models are created for the new designs. Simulation results on the current density and the divergence of the total flux, which is responsible for electromigration, are extracted based on the coupled field solutions. The results show that the new designs reduce the maximum divergence of the flux and current density by as much as 42%. New Design A proves to be more effective than Design B.

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